

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1    1. An interconnection wiring system containing at least one  
2    capacitor comprising:

3    a substrate having a planar upper surface of insulating areas and  
4    conductive regions therein,

5    a first level of interconnection wiring interconnecting said  
6    conductive regions,

7    said first level of interconnection wiring further including a  
8    patterned region to form the lower electrode of a capacitor,

9    a first dielectric layer formed over said lower electrode,

10   a top electrode formed over said first dielectric layer to form the  
11   top electrode of said capacitor, said top electrode having a  
12   perimeter interior to the perimeter of said first dielectric layer,

13   a second dielectric layer formed over said first level of  
14   interconnection wiring, over said first dielectric layer and over  
15   said top electrode, said second dielectric layer being  
16   substantially thicker than said first level of interconnection  
17   wiring, said first dielectric layer and said top electrode;

18   said second dielectric layer having an upper surface and having  
19   vias filled with conductive material to said upper surface and in  
20   contact with regions of said first level of interconnection wiring

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21 and said top electrode, and  
22 a second level of interconnection wiring interconnecting said vias  
23 filled with conductive material.

1 2. The interconnection wiring system of claim 1 wherein said lower  
2 electrode has an upper surface of titanium nitride.

1 3. The interconnection wiring system of claim 1 wherein said top  
2 electrode has a lower surface of titanium nitride.

1 4. The interconnection wiring system of claim 2 wherein said top  
2 electrode has a lower surface of titanium nitride.

1 5. An interconnection wiring system containing at least one  
2 capacitor comprising:  
3 a substrate having a planar upper surface of insulating and  
4 conductive regions therein.  
5 a first level of interconnection wiring interconnecting said  
6 conductive regions.  
7 a first dielectric layer formed over said first level of  
8 interconnection wiring,  
9 said first dielectric layer having an upper surface and having vias  
10 therein filled with conductive material to said upper surface and  
11 in contact with regions of said first level of interconnection  
12 wiring.  
13 at least one of said vias having dimensions to form said lower  
14 electrode of a capacitor.

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15 a second dielectric layer formed over said lower electrode and  
16 extending beyond the perimeter of said lower electrode, and

17 a second level of interconnection wiring interconnecting the vias  
18 filled with conductive material and formed over the second  
19 dielectric layer to form said top electrode of said capacitor.

1 6. The interconnection wiring system of claim 1 wherein said lower  
2 electrode has an upper surface of titanium nitride.

1 7. The interconnection wiring system of claim 1 wherein said top  
2 electrode has a lower surface of titanium nitride.

1 8. The interconnection wiring system of claim 6 wherein said top  
2 electrode has a lower surface of titanium nitride.

1 9. A method for forming an interconnection wiring system  
2 containing at least one capacitor comprising the steps of:

3 selecting a substrate having a planar upper surface of insulating  
4 areas and conductive regions thereon,

5 forming a first level of interconnection wiring interconnecting  
6 said conductive regions, and

7 forming a patterned region to form the lower electrode of a  
8 capacitor.

9 forming a first dielectric layer over said lower electrode.

10 forming a top electrode over said first dielectric layer to form  
11 the top electrode of said capacitor wherein said top electrode has  
12 a perimeter interior to the perimeter of said first dielectric

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13 layer.

14 forming a second dielectric layer over said first level of  
15 interconnection wiring, over said first dielectric layer and over  
16 said top electrode, wherein said second dielectric layer being  
17 substantially thicker than said first level of interconnection  
18 wiring, said first dielectric layer and said top electrode.

19 forming vias in the upper surface of said second dielectric layer  
20 down to regions of said first level of interconnection wiring and  
21 to said top electrode and filling vias with conductive material to  
22 said upper surface, and

23 forming a second level of interconnection wiring interconnecting  
24 said vias filled with conductive material.

1 10. The method of claim 9 further including the step of forming  
2 a lower electrode having an upper surface of titanium nitride.

1 11. The method of claim 9 further including the step of forming  
2 a top electrode having a lower surface of titanium nitride.

1 12. The method of claim 10 further including the step of  
2 forming a top electrode having a lower surface of titanium nitride.

1 13. A method of forming an interconnection wiring system  
2 containing at least one capacitor comprising the steps of:  
3 selecting a substrate having a planar upper surface of insulating  
4 and conductive regions therein.  
5 forming a first level of interconnection wiring interconnecting  
6 said conductive regions.

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7 forming a first dielectric layer over said first level of  
8 interconnection wiring, wherein

9 forming vias in the upper surface of said first dielectric layer  
10 down to regions of said first level of interconnection wiring and  
11 filling vias therein with conductive material to said upper  
12 surface, and

13 at least one of said vias having dimensions to form said lower  
14 electrode of a capacitor.

15 forming a second dielectric layer over said lower electrode and  
16 extending beyond the perimeter of said lower electrode, and

17 forming a second level of interconnection wiring interconnecting  
18 the vias filled with conductive material and formed over the second  
19 dielectric layer to form said top electrode of said capacitor.

1 14. The method of claim 13 further including the step of  
2 forming a lower electrode having an upper surface of titanium  
3 nitride.

1 15. The method of claim 13 further including the step of  
2 forming a top electrode having a lower surface of titanium nitride.

1 16. The method of claim 14 further including the step of  
2 forming a top electrode having a lower surface of titanium nitride.

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